SCOPE OF CLAIM

[1] An integrated circuit production method characterized by: a step of producing a trial integrated circuit based on pattern information for a trial production, without using a photomask, under a common design circumstance which can be utilized in both a photomaskless step of producing an integrated circuit based on pattern information without using a photomask and a photomask step of producing an integrated circuit based on pattern information with using a photomask, with the pattern information for the trial production complying with both the photomaskless step and the photomask step; a step of preparing a common pattern information by evaluating the trial integrated circuit and by improving, if necessary, the pattern information for the trial production in accordance with results of the evaluation; and a step of producing a photomask for a mass production by carrying out a formal conversion of the common pattern information, if necessary, without improving the common pattern information.

[2] The integrated circuit production method as set forth in claim 1, characterized in that said common design circumstance is constituted as a design circumstance, including design tools, such as, an EDA (electronic design automation) software, an inspection software, a cell library, IP (intellectual property), an OPC (optical and process correction) processing software and so on necessary for an integrated circuit production, so as to be commonly utilized in both said photomaskless step and said photomask step.

[3] The integrated circuit production method as set forth in claim 1, characterized in that said trial integrated circuit is produced on the same wafer based on the pattern information which is featured by different integrated circuits, integrated circuits having the same functions and parameters for requirements, or a combination of some of these integrated

circuits, without using the photomask.

[4] The integrated circuit production method as set forth in claim 3, characterized in that a mass production of chips is carried out by the photomask apparatus, using a photomask which is produced based on pieces of common pattern information which are concerned with respective chips assigned on the same wafer in accordance with external demands.

[5] An integrated circuit design assistance program characterized in that a computer functions as a conversion means for converting design information, prepared through the intermediary of an integration circuit function design and/or a logic design, into pattern information which satisfies both a pattern characteristic of a photomaskless apparatus for producing an integrated circuit based on pattern information without using a photomask and a pattern characteristic of a photomask apparatus for producing an integrated circuit by using a photomask based on pattern information.

[6] The integrated circuit design assistance program as set forth in claim 5, characterized in that said conversion means carries out the conversion of the design information into the pattern information by using a cell library, which comprises a congregation composed of pattern components which satisfies both the pattern characteristic of the photomaskless apparatus and the pattern characteristic of the photomask apparatus.

[7] An integrated circuit design assistance apparatus characterized by a conversion means for converting design information, prepared through the intermediary of an integration circuit function design and/or a logic design, into pattern information which satisfies both a pattern characteristic of a photomaskless apparatus for producing an integrated circuit based on pattern information without using a photomask and a pattern characteristic of a photomask apparatus for producing an integrated circuit by using a photomask based on pattern

information.

[8] The integrated circuit design assistance apparatus as set forth in claim 5, characterized in that said conversion means carries out the conversion of the design information of the pattern information by using a cell library, which comprises a congregation composed of pattern components which satisfies the pattern characteristic of the photomaskless apparatus and the pattern characteristic of the photomask apparatus.

[9] An integrated circuit design system comprising: either an integrated circuit design assistance apparatus obtained by installing the integrated circuit design assistance program of claim 5 or 6 in a computer or an integrated circuit design assistance apparatus as set forth in claim 7 or 8; said photomaskless apparatus; and said photomask apparatus,

characterized by the fact that said integrated circuit design assistance apparatus outputs either pattern information or similar pattern information, allowed to be input to the photomaskless apparatus, to the photomaskless apparatus, by the fact that the photomaskless apparatus produces a trial integrated circuit based on either the pattern information or the similar pattern information, by the fact that the trial integrated circuit is evaluated to prepare common pattern information, with the common pattern information being improved, if necessary, and by the fact that a mass production of chips is carried out by the photomask apparatus, using a photomask based on the common pattern information.

[10] The integrated circuit design system as set forth in claim 9, characterized in that said conversion means carries out the conversion of the design information into the pattern information so that a juncture, caused by a width of an electron beam of an electron beam direct drawing apparatus, departs from an active area.

[11] The integrated circuit design system as set forth in claim

9, characterized in that said conversion means further converts the converted pattern information into pattern information subjected to an OPC processing for the photomask apparatus.

[12] The integrated circuit design system as set forth in claim 9, characterized in that said photomaskless apparatus produces trial integrated circuits on the same wafer based on either pieces of pattern information or similar pieces of pattern information allowed to be input to the photomaskless apparatus.

[13] The integrated circuit design system as set forth in claim 12, characterized in that the mass production of the chips is carried out by the photomask apparatus, using the photomask which are produced based on pieces of common pattern information which are concerned with respective chips assigned on the same wafer in accordance with external demands.

[14] A block mask used in a block exposure carried out by a photomaskless apparatus for producing an integrated circuit without using a photomask, characterized in that the block mask is formed with a plurality of blocks, sides of which have different lengths.

[15] A block mask used in a block exposure carried out by a photomaskless apparatus for producing an integrated circuit without using a photomask, characterized in that the block mask is formed with a plurality of rectangular blocks, sizes of which are different from each other.

[16] The block mask as set forth in claim 14 or 15, characterized in that, when each of the blocks is shaped as a rectangular block, a long side and/or a short side of the rectangular block have lengths featured by a multiple of the minimum wiring pitch unit.

[17] The block mask as set forth in claim 14 or 15, characterized in that short sides of the blocks have the same length, and long sides of the blocks have different lengths.

[18] The block mask as set forth in claim 14 or 15, characterized in that the block mask has a vertically-lengthened block area

in which the blocks are arranged so that the long sides of the blocks extend in a vertical direction of the block mask, and a horizontally-lengthened block area in which the blocks are arranged so that the long sides of the blocks extend in a horizontal direction of the block mask.

[19] A photomaskless apparatus using a block mask as set forth in claim 14 or 15, characterized by a means for deforming a shape of beam, which is emitted during a block exposure, into either an elongatedly rectangular shape or an elongatedly elliptic shape.

[20] A photomaskless apparatus using a block mask as set forth in claim 14 or 15, characterized in that a block is scanned with an emitted beam during an block exposure, while a shape of the beam is maintained.

[21] A photomaskless apparatus using a block mask as set forth in claim 14 or 15, characterized in that a block is irradiated with a plurality of beams which are arranged in a longitudinal direction of the block during an block exposure.

[22] A photomaskless apparatus using the block mask, as set forth in claim 21, characterized in that the block is divided at regular intervals into sections at the number of beams which are longitudinally emitted, and the divided sections are irradiated and scanned with the respective beams.

[23] An integrated circuit production method characterized by: a step of producing cells in which pattern components corresponding to the same exposure step are identified to each other among cells of a cell library which are different from each other in a function and a capability, without exerting influence on an operation; a step of registering the produced cells in the cell library; and a step of carrying out a block exposure, using a block mask on which patterns are formed based on the cell library.

[24] An integrated circuit production method characterized by;

a step of preparing a cell of a 1-input gate, composed of a 1-input N-type transistor and a 1-input P-type transistor, as a basic cell unit in a cell library for a CMOS semiconductor device; a step of registering a cell of an N-input gate, composed of pattern components each forming a basic cell of the 1-input gate, in the cell library; and a step of carrying out an block exposure, using a block mask on which patterns are formed based on the cell library.

[25] The integrated circuit production method as set forth in claim 1, characterized by: a step of producing cells in which pattern components corresponding to the same exposure step are identified to each other among cells of a cell library which are different from each other in a function and a capability, without exerting influence on an operation; a step of registering the produced cells in the cell library; and a step of carrying out a block exposure, using a block mask on which patterns are formed based on the cell library.

[26] The integrated circuit production method as set forth in any one of claims 23 through 25, characterized in that the block exposure is carried out, using the block mask as set forth in claim 14 or 15.